CECS 225

Homework 6

Sotheanith Sok

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|  | lw $2, 80($0) | | | | | | |
| **RegDst**  **Mux** | **Register**  **File** | **Sign**  **Extender** | **ALU**  **Source**  **Mux** | **ALU**  **Decoder**  **Signals** | **ALU Data**  **Signals** | **MemtoReg**  **Mux** |
| Data Input Signals | *Instr[20:16]* | *Instr[25:21]* | *Instr[15:0]* | *WriteData* | *Funct* | *SrcA* | *ALUResult* |
| **2** | **0** | **16’h80** | **32’h7** | **X** | **32’h0** | **32’h80** |
| *Instr[15:11]* | *Instr[20:16]* |  | *SignImm* |  | *SrcB* | *ReadData* |
| **0** | **2** | **32’h80** | **32’h80** | **32’h80** |
|  | *WriteReg* |  |  |  |
| 2 |
| *WriteData* |
| **32’h80** |
| Control  Signals | *RegDst* | *RegWrite* |  | *ALUSrc* | *ALUOp* | *ALUControl* | *MemtoReg* |
| **1’b0** | **1’b1** | **1’b1** | **0** | **2** | **1’b1** |
| Output  Signals | *WriteReg* | *SrcA* | *SignImm* | *SrcB* | *ALUControl* | *Zero* | *Result* |
| **2** | **32’h0** | **32’h80** | **32’h80** | **2** | **0** | **32’h80** |
|  | *WriteData* |  |  |  | *ALUResult* |  |
| **32’h7** | **32’h80** |

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|  | slt $4, $3, $4  4 | | | | | | |
| **RegDst**  **Mux** | **Register**  **File** | **Sign**  **Extender** | **ALU**  **Source**  **Mux** | **ALU**  **Decoder**  **Signals** | **ALU Data**  **Signals** | **MemtoReg**  **Mux** |
| Data Input Signals | *Instr[20:16]* | *Instr[25:21]* | *Instr[15:0]* | *WriteData* | *Funct* | *SrcA* | *ALUResult* |
| **4** | **3** | **16’h202A** | **32’h0** | **42** | **32’hC** | **32’h0** |
| *Instr[15:11]* | *Instr[20:16]* |  | *SignImm* |  | *SrcB* | *ReadData* |
| **4** | **4** | **32’h202A** | **32’h0** | **32’h0** |
|  | *WriteReg* |  |  |  |
| **4** |
| *WriteData* |
| **32’h0** |
| Control  Signals | *RegDst* | *RegWrite* |  | *ALUSrc* | *ALUOp* | *ALUControl* | *MemtoReg* |
| **1’b1** | **1’b1** | **1’b0** | **2** | **7** | **1’b0** |
| Output  Signals | *WriteReg* | *SrcA* | *SignImm* | *SrcB* | *ALUControl* | *Zero* | *Result* |
| **4** | **32’hC** | **32’h202A** | **32’h0** | **7** | **0** | **32’h0** |
|  | *WriteData* |  |  |  | *ALUResult* |  |
| **32’h0** | **32’h0** |

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|  | sw $7, 68($3) | | | | | | |
| **RegDst**  **Mux** | **Register**  **File** | **Sign**  **Extender** | **ALU**  **Source**  **Mux** | **ALU**  **Decoder**  **Signals** | **ALU Data**  **Signals** | **MemtoReg**  **Mux** |
| Data Input Signals | *Instr[20:16]* | *Instr[25:21]* | *Instr[15:0]* | *WriteData* | *Funct* | *SrcA* | *ALUResult* |
| **7** | **3** | **16’h44** | **32’h7** | **X** | **32’hC** | **32’h50** |
| *Instr[15:11]* | *Instr[20:16]* |  | *SignImm* |  | *SrcB* | *ReadData* |
| **0** | **7** | **32’h44** | **32’h44** | **32’X** |
|  | *WriteReg* |  |  |  |
| **X** |
| *WriteData* |
| **32’hX** |
| Control  Signals | *RegDst* | *RegWrite* |  | *ALUSrc* | *ALUOp* | *ALUControl* | *MemtoReg* |
| **1’bX** | **1’b0** | **1’b1** | **0** | **2** | **1’bX** |
| Output  Signals | *WriteReg* | *SrcA* | *SignImm* | *SrcB* | *ALUControl* | *Zero* | *Result* |
| **X** | **32’hC** | **32’h44** | **32’h44** | **2** | **Binary** | **32’hX** |
|  | *WriteData* |  |  |  | *ALUResult* |  |
| **32’h7** | **32’h50** |

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|  | beq $5, $7, 0x000A | | | | | | |
| **RegDst**  **Mux** | **Register**  **File** | **Sign**  **Extender** | **ALU**  **Source**  **Mux** | **ALU**  **Decoder**  **Signals** | **ALU Data**  **Signals** | **MemtoReg**  **Mux** |
| Data Input Signals | *Instr[20:16]* | *Instr[25:21]* | *Instr[15:0]* | *WriteData* | *Funct* | *SrcA* | *ALUResult* |
| **7** | **5** | **16’hFFF9** | **32’h3** | **X** | **32’hB** | **32’h8** |
| *Instr[15:11]* | *Instr[20:16]* |  | *SignImm* |  | *SrcB* | *ReadData* |
| **31** | **7** | **32’hFFF9** | **32’h3** | **32’’h8** |
|  | *WriteReg* |  |  |  |
| **X** |
| *WriteData* |
| **32’hX** |
| Control  Signals | *RegDst* | *RegWrite* |  | *ALUSrc* | *ALUOp* | *ALUControl* | *MemtoReg* |
| **1’bX** | **1’b0** | **1’b0** | **1** | **6** | **1’bX** |
| Output  Signals | *WriteReg* | *SrcA* | *SignImm* | *SrcB* | *ALUControl* | *Zero* | *Result* |
| **X** | **32’hB** | **32’hFFF9** | **32’h3** | **6** | **0** | **32’hX** |
|  | *WriteData* |  |  |  | *ALUResult* |  |
| **32’h3** | **32’h8** |

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|  | addi $7, $3, -9 | | | | | | |
| **RegDst**  **Mux** | **Register**  **File** | **Sign**  **Extender** | **ALU**  **Source**  **Mux** | **ALU**  **Decoder**  **Signals** | **ALU Data**  **Signals** | **MemtoReg**  **Mux** |
| Data Input Signals | *Instr[20:16]* | *Instr[25:21]* | *Instr[15:0]* | *WriteData* | *Funct* | *SrcA* | *ALUResult* |
| **7** | **3** | **16’hFFF7** | **32’h3** | **X** | **32’hC** | **32’h100000003** |
| *Instr[15:11]* | *Instr[20:16]* |  | *SignImm* |  | *SrcB* | *ReadData* |
| **31** | **7** | **32hFFF7** | **32’FFF7** | **32’h100000003** |
|  | *WriteReg* |  |  |  |
| **7** |
| *WriteData* |
| **32’h100000003** |
| Control  Signals | *RegDst* | *RegWrite* |  | *ALUSrc* | *ALUOp* | *ALUControl* | *MemtoReg* |
| **1’b0** | **1’b1** | **1’b1** | **0** | **2** | **1’b0** |
| Output  Signals | *WriteReg* | *SrcA* | *SignImm* | *SrcB* | *ALUControl* | *Zero* | *Result* |
| **7** | **32’hC** | **32’hFFF7** | **32’FFF7** | **2** | **0** | **32’h100000003** |
|  | *WriteData* |  |  |  | *ALUResult* |  |
| **32’h3** | **32’h100000003** |